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(54) Amplifier arrangement.

(57) A signal voltage applied between the input terminals (3, 4) is converted by means of a differential amplifier (T_7-T_{10}) into two phase-opposed signal currents which are inverted by means of a differential-to-single-ended converter (10) into a single-ended signal current. The converter (10) comprises a first and a second transistor (T_1, T_2) with a common gate electrode and a third and a fourth transistor (T_3,T_4) also with a common gate electrode, whilst the drain electrode of the third transistor (T_3) is connected to the common gate electrode of the first and the second transistor (T_1, T_2). The common gate electrode of the third and the fourth transistor (T_3, T_4) is maintained at a voltage which is equal to the sum of one threshold voltage and two saturation voltages by means of a fifth transistor (T_5) whose gate electrode is connected to the drain electrode and to a bias current source (I_2). The output (5) of the amplifier can be driven by means of this converter (10) up to two saturation voltages of the negative supply terminal (1).

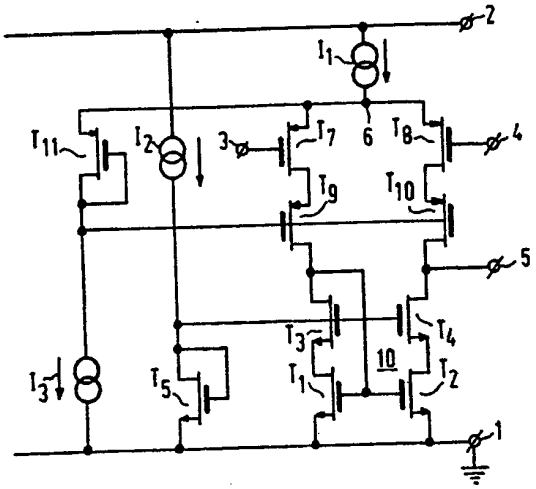


FIG.1

EP 0 308 000 A1

Amplifier arrangement.

The invention relates to an amplifier arrangement comprising a differential amplifier having two input terminals for receiving an input voltage and a differential-to-single-ended converter having an output terminal for supplying an output current, said converter including a first and a second transistor of a first conductivity type whose source electrodes are coupled to a first supply terminal and whose gate electrodes are coupled together, and a third and a fourth transistor of the first conductivity type arranged in cascade with the first and the second transistor, respectively, and having their gate electrodes coupled together.

An amplifier arrangement of this type can be generally used as an operational amplifier having a relatively high gain and a relatively large bandwidth. Such an arrangement can be particularly used in video circuits, switched capacitor circuits and sample and hold circuits.

Such an amplifier arrangement is known from the book "Analysis and Design of Analog Integrated Circuits" P.R. Gray; R.G. Meyer, 1984 John Wiley and Sons Inc., page 753, fig. 12.38.

In this known arrangement the differential-to-single-ended converter is constituted by an improved Wilson current mirror in which the gate electrodes of both the first transistor and the third transistor are connected to the drain electrode.

This arrangement has the drawback that the output voltage swing of the amplifier arrangement is comparatively small. In fact, the drain electrode of the fourth transistor connected to the output can only be driven up to the sum of one threshold voltage and two saturation voltages with respect to the negative supply terminal.

It is therefore an object of the invention to provide an amplifier arrangement having a larger output voltage swing than the known arrangement. According to the invention an amplifier arrangement ofa type described in the opening paragraph is characterized in that the gate electrode of the first transistor is coupled to the drain electrode of the third transistor and in that the arrangement also includes a bias circuit for biassing the gate electrodes of the thirdand the fourth transistor at a voltage which is substantially equal to the sum of one threshold voltage and two saturation voltages. In the arrangement according to the invention the output can be driven up to two saturation voltages with respect to the negativ supply terminal. As compared with the known arrangement this results in an increase of the output voltage swing by one threshold voltage which is usually substantially 1 Volt. This leads to a considerable improvement of the output voltage swing, particularly at low supply voltages.

A first embodiment of an amplifier arrangement according to the invention may be characterized in that the bias circuit includes a fifth transistor of the first conductivity type whose source electrode is coupled to the first supply terminal and whose gate electrode is coupled to the common gate electrode of the third and the fourth transistor and to its drain electrode which is coupled to a second supply terminal by means of a first current source. The gate-source voltage of the fifth transistor is biassed by means of the first current source at a voltage which is equal to the sum of the threshold voltage and the saturation voltage of the fourth transistor and the saturation voltage of the second transistor so that the output can be driven up to at least two saturation voltages.

A second embodiment of an amplifier arrangement may be characterized in that a sixth transistor of the first conductivity type is arranged in series with the fifth transistor, the gate electrode of the fifth transistor being coupled to the gate electrode and to the drain electrode of the sixth transistor.

A third embodiment of an amplifier arrangement according to the invention may be characterized in that the differential amplifier includes a seventh and an eighth transistor of a second conductivity type opposite to the first conductivity type whose gate electrodes are coupled to the input terminals and whose source electrode are coupled to a common terminal which is coupled by means of a second current source to a second supply terminal, and a ninth and a tenth transistor of the second conductivity type which are arranged in cascade with the seventh and the eighth transistor, respectively. This embodiment may be further characterized in that the gate electrodes of the ninth and the tenth transistor are coupled together and in that an eleventh transistor of the second conductivity type is arranged between the common terminal of the source electrodes of the seventh and the eighth transistor and the common gate electrode of the ninth and the tenth transistor, the drain electrode of said eleventh transistor being connected to its gate electrode and to the first supply terminal by means of a third current source. The common gate electrode of the ninth and the tenth transistor is biassed by means of the eleventh transistor at a substantially fixed voltage with respect to the common terminal of the source electrodes of the seventh and eighth transistors.

A further embodiment may be characterized in that a twelfth transistor of the first conductivity type is arranged in series with the elev nth transistor,

said twelfth transistor having its source electrode coupled to the common gate electrod of the ninth and the tenth transistor and having its gate electrode coupled to the second supply terminal. Due to the twelfth transistor the voltage difference between the common terminal of the source electrodes of the seventh and the eighth transistor and the common gate electrode of the ninth and the tenth transistor remain substantially constant over a large input d. c. voltage range.

A suitable further embodiment may be characterized in that the third current source is constituted by a thirteenth transistor of the first conductivity type whose source electrode is coupled to the first supply terminal and whose gate electrode is coupled to the gate electrode of the fifth transistor.

A fourth embodiment of an a mplifier arrangement according to the invention may be characterized in that the arrangement is formed as an integrated circuit on a substrate of a first conductivity type in which the seventh and the eight transistor are arranged in a zone of a second conductivity type which is connected to the second supply terminal and in which the ninth and the tenth transistor are arranged in separate zones of the second conductivity type which are connected to the source electrodes of the seventh and the eighth transistor, respectively, and in that the gate electrodes of the ninth and the tenth transistor are connected to the gate electrodes of the sevent and the eighth transistor, respectively. In this embodiment the so-called back-gate effect is used according to which the threshold voltage of a transistor increases as the bulk voltage increases. By connecting the zone in which the seventh and the eighth transistor are formed to a higher voltage than the zones in which the ninth and the tenth transistor are formed, the seventh and the eighth transistor acquire a higher threshold voltage than the ninth and the tenth transistor. This difference is so large that the gate electrodes of the ninth and the tenth transistor can be connected without any problem to the gate electrodes of the seventh and the eighth transistor.

A fifth embodiment of an amplifier arrangement according to the invention in which this back-gate effect is also used may be characterized in that the arrangement is formed as an integrated circuit on a substrate of a first conductivity type inwhich the seventh and the eighth transistor are arranged in a zone of a second conductivity type which is connected to the second supply terminal and in which the ninth and the tenth transistor are arranged in a common zone of the second conductivity type which is connected to the common t rminal of the source electrodes of the sev nth and the eighth transistor, and in that the gat electrodes of th ninth and the tenth transistor are connected to the gate electrodes of the seventh and the eighth transistor, respectively.

A fifth embodiment in which this effect is als used may be characterized in that the arrangement is formed as an integrated circuit on a substrate of a first conductivity type in which the seventh and the eighth transistor are arranged in a zone of a second conductivity type which is connected to the second supply terminal and in which the ninth and the tenth transistor are arranged in a common zone of the second conductivity type which is connected to the common terminal of the source electrodes of the seventh and the eighth transistor, and in that the gate electrode of the ninth transistor is connected to the gate electrode of the tenth transistor and to the gate electrode of the seventh transistor.

The invention will now be described in greater detail by way of example with reference to the accompanying drawings in which

Fig. 1 shows a first embodiment of an amplifier arrangement according to the invention,

Fig. 2 shows a second embodiment of an amplifier arrangement according to the invention;

Fig. 3 shows a third embodiment of an amplifier arrangement according to the invention;

Fig. 4 shows a fourth embodiment of an amplifier arrangement according to the invention;

Fig. 5 shows a fifth embodiment of an amplifier arrangement according to the invention, and

Fig. 6 shows a sixth embodiment of an amplifier arrangement according to the invention.

Corresponding components have the same reference numerals in these Figures.

Fig. 1 shows a first embodiment of an amplifier arrangement according to the invention. It comprises two P-channel transistors T_7 and T_8 arranged as a differential pair whose common source terminal 6 is connected to the positive supply terminal 2 by means of a current source I_1. The gate electrodes of transistors T_7 and T_8 are connected to input terminals 3 and 4 for receiving an input voltage. Two P-channel transistors T_9 and T_{10} are arranged in cascode with transistors T_7 and T_8, respectively. The transistors T_9 and T_{10} have a common gate electrode which is maintained at a substantially fixed voltage with respect to the so-called common-mode voltage at the common source terminal 6 by means of a P-channel transistor T_{11} whose drain electrode is connected to the gate electrode and to the negative supply terminal 1, in this embodiment ground, by means of a current sourc I_3.

A signal voltage applied between the input terminals 3 and 4 is converted by the differential amplifier T_7-T_{10} into two phase opposed signal currents which can in principle be taken from the

drain electrodes of the transistors T_9 and T_{10}. As is known,the cascode transistors T_9 and T_{10} increase the bandwidth of the amplifier arrangement because the Miller effect of the drain-gate capacitance of the transistors T_7 and T_8 is eliminated. Besides, the output impedance and hence the gain of the amplifier arrangement is increased thereby.

The drain electrode of transistor T_9 is coupled to both the drain electrode of transistor T_{10} and to the output terminal 5 of the amplifier arrangement by means of a differential-to-single-ended converter 10 which converts the differential signal currents in the drain leads of transistors T_9 nand T_{10} into a single-ended output current at output terminal 5. The converter 10 has two N-channel transistors T_1 and T_2 whose source electrodes are connected to the supply terminal 1 and whose gate electrodes are connected together and to the drain electrode of transistors T_9. Two N-channel transistors T_3 and T_4 are arranged in cascode with transistors T_1 and T_2, respectively. The gate electrodes of these transistors are connected together and are biassed at a fixed voltage with respect to ground by means of a bias circuit. This circuit is constituted by an N-channel transistor T_5 whose source electrode is connected to ground and whose gate electrode is connected to the drain electrode and to the common gate electrode of transistors T_3 and T_4. The drain electrode of transistor T_5 is connected to the positive supply terminal 2 by means of a current source I_2. The transistors T_1 and T_2 of the converter 10 constitute a current mirror which mirrors the current flowing through transistor T_4. The d.c. component therein compensates the d.c. component of the current through transistor T_{10}, whilst the phase-opposed signal currents result in an output signal current which is twice as large. Due to the cascode transistors T_4 and T_{10} the amplifier arrangement acquires a high output impedance and hence a large gain. Moreover, the cascode transistors T_4 and T_{10} eliminate the Miller effect of the drain-gate capacitance which is otherwise present between the output terminal 5 and the gate electrode of transistor T_2 and the gate electrode of transistor T_8, respectively. Consequently the amplifier arrangement acquires a large bandwidth. The transistors T_3 and T_9 render the arrangement symmetrical and decrease the d.c. offset at the output.

The current intensity of the current source I_2 and the dimensions of transistor T_5 are chosen to be such that the gate-source voltage of transistor T_5 is substantially equal to the sum of the threshold voltage and the saturation voltage of transistor T_4 and the saturation voltage of transistor T_2. The saturation voltage is the minimum drain- source voltage which is required to bias a transistor in its saturation range. Since the gate-source voltage of transistor T_4 is equal to th sum of its threshold voltage and its saturation voltage, the voltage at the source electrode of transistor T_4 is then at least equal to the saturati n voltage of transistor T_2 so that the voltage at the output terminal 5 can b - come at least equal to the sum of the saturation voltages of transistors T_2 and T_4. The output terminal 5 may therefore be driven up to two saturation voltages, that is to say, up to substantially 400 mV of the negative supply terminal 1 without a loss of gain. As compared with the known arrangement this is an increase of the output voltage swing by one threshold voltage of approximately 1 V, which is a considerable improvement, particularly at low supply voltages.

Fig. 2 shows a second embodiment of an amplifier arrangement according to the invention. The bias circuit for biassing the common gate electrode of transistors T_3 and T_4 now includes an N-channel transistor T_6 which is arranged in series with transistor T_5 and whose drain electrode is connected to its gate electrode and to the gate electrode of transistor T_5. In the arrangement of Fig. 1 transistor T_5 will be generally biassed at a lower current than the transistors T_2 and T_4 in order to obtain a low dissipation. To realise the desired bias voltage the channel length of transistor T_5 should be larger than that of transistors T_2 and T_4. The spread in the channel length of the transistors occurring due to process variations thereby influences the gate-source voltage of transistor T_5 and hence the bias voltage in a different way than the gate-source voltages of transistor T_4 and transistor T_2. By splitting transistor T_5 into two transistors T_5 and T_6 each having shorter channel lengths, the bias voltage variations occurring due to process variations are substantially equal to the variations of the voltages of the transistors T_2 and T_4 so that the minimum output voltage swing has become substantially independent of these process variations.

In this embodiment current source I_3 is formed advantageously by an N-channel transistor T_{13} whose source is connected to ground terminal 1 and whose gate electrode is connected to the gate electrode of transistor T_5 which is at a fixed voltage with respect to ground.

Fig. 3 shows a third embodiment of an amplifier arrangement according to the invention. In this embodiment the series arrangement of a P-channel transistor T_{11} whose gate electrode is connected to the drain electrode and an N-channel transistor T_{12} whose gate electrode is connected to the positive supply terminal 2 is arranged between the common source terminal 6 and the common gate electrode of the transistors T_9 and T_{10}. The common gate electrode of the transistors T_9 and T_{10} is maintained by this arrangement at a fixed voltage with respect to the terminal 6 over a large input d.c. voltage range. In face, the gate-source

voltage variations of transistor T_{11} occurring in th case of input d.c. voltage variations are compensated by oppositely occurring variations of the drain-source voltage of transistor T_{12} so that the sum of these voltages remains substantially constant.

Fig. 4 shows a fourth embodiment of an amplifier arrangement according to the invention. In this embodiment it is not necessary to use a separate bias circuit to bias the common gate electrode of the transistors T_9 and T_{10} at a substantially fixed voltage with respect to the terminal 6, but the gate electrodes of transistors T_9 and T_{10} are connected to the gate electrodes of transistors T_7 and T_8, respectively. In this arrangement use is made of the so-called back-gate effect which causes the threshold voltage of a transistor to increase as the voltage between the source electrode and the bulk material in which the transistor is formed increases. In this embodiment the arrangement is integrated on a P-type substrate. The transistors T_7 and T_8 are formed in an N-well 20 which is connected to the positive supply terminal 2 and the transistors T_9 and T_{10} are formed in N-wells 30 and 40 which are connected to the source electrode of the relevant transistor. Since the source-bulk voltage of transistors T_7 and T_8 is high and that of transistors T_9 and T_{10} is zero, the threshold voltage of transistors T_7 and T_8 is larger than that of transistors T_9 and T_{10}. The difference between these threshold voltages is present between the source and drain electrodes of transistors T_7 and T_8. Although the source-bulk voltage of transistors T_7 and T_8 is dependent on the input d.c. voltage, this voltage difference is sufficiently large over a relatively large range to drive transistors T_7 and T_8 into saturation so that these transistors can convey a sufficiently large current. The threshold voltage of transistors T_7 and T_8 is, for example substantially equal to 1.4 V over a relatively large range, whilst the threshold voltage of transistors T_9 and T_{10} is equal to 1.0 Volt.

Fig. 5 shows a fifth embodiment of an amplifier arrangement according to the invention. In this embodiment the transistors T_9 and T_{10} are not arranged in separate N-wells but in one common N-well 40 which is connected to the common source terminal 6. The gate electrodes of transistors T_9 and T_{10} are again connected to the gate electrodes of transistors T_7 and T_8. In this embodiment both the source-bulk voltage of the transistors T_7 and T_8 and the source-bulk voltage of the transistors T_9 and T_{10} is dependent on the input d.c. voltage. the source-bulk voltage of transistors T_7 and T_8 is then larger than th source-bulk voltage of the transistors T_9 and T_{10} so that the threshold voltage of transistors T_7 and T_8 is always larger than that of transistors T_9 and T_{10}. The difference between these voltages is present between the source and drain electrodes of transistors T_7 and T_8 and is larger than the saturation voltage of these transistors over a relatively reasonably large range of the input d.c. voltage so that these transistors can convey a relatively large current. The arrangement of Fig. 5 is built up very symmetrically. This arrangement is very suitable for use as a buffer amplifier.

Fig. 6 shows a sixth embodiment of an amplifier arrangement according to the invention. In this embodiment the transistors T_9 and T_{10} are arranged in a common N-well 40 which is connected to the common terminal 6 of the source electrodes of the transistors T_7 and T_8. The gate electrodes of the transistors T_9 and T_{10} are interconnected and are connected to the gate electrode of input transistor T_7. This arrangement substantially has the same properties as the arrangement of Fig. 5, but it is built up less symmetrically. The amplifier arrangement of Fig. 6 is particularly suitable for use in an inverting amplifier in which a first capacitor is connected to the input 4 and a second capacitor is arranged between the input 4 and the output 5. If the arrangement of Fig. 5 is used in such an amplifier, the drain-gate capacitance of transistor T_{10} influences the gain. When using the arrangement of Fig. 6 in such an amplifier, this effect does not occur and the gain is only determined by the first and the second capacitor.

The invention is not limited to the embodiments shown and many variations within the scope of the invention are possible to those skilled in the art. The bias circuit for biassing the common gate electrode of the transistors T_3 and T_4 may be formed in any other way than in the manners shown, provided that this voltage is at least equal to the sum of one threshold voltage and two saturation voltages. The differential amplifier may also be built up in any other way than in the manner shown. In the embodiments of Fig. 5 and 6 the common N-well of the transistors T_9 and T_{10} may in principle also be connected to the source electrode of transistor T_9. Finally, the amplifier arrangement may of course also be formed with transistors of the opposite conductivity type.

Claims

1. An amplifier arrangement comprising a differential amplifier having two input terminals for receiving an input voltage and a differential-to-single-ended converter having an output terminal for supplying an output current, said converter including a first and a second transistor of a first conductivity type whose source electrodes are coupled to a first supply terminal and whose gate

electrodes are coupled together, and a third and a fourth transistor of the first conductivity type arranged in cascode with the first and the second transistor, respectively, and having their gate electrodes coupled together, characterized in that the gate electrode of the first transistor is coupled to the drain electrode of the third transistor and in that the arrangement also includes a bias circuit for biassing the gate electrodes of the third and the fourth transistor at a voltage which is substantially equal to the sum of one threshold voltage and two saturation voltages.

2. An amplifier arrangement as claimed in Claim 1, characterized in that the bias circuit includes a fifth transistor of the first conductivity type whose source electrode is coupled to the first supply terminal and whose gate electrode is coupled to the common gate electrode of the third of the fourth transistor and to its drain electrode which is coupled to a second supply terminal by means of a first current source.

3. An amplifier arrangement as claimed in Claim 2, characterized in that a sixth transistor of the first conductivity type is arranged in series with the fifth transistor, the gate electrode of the fifth transistor being coupled to the gate electrode and to the drain electrode of the sixth transistor.

4. An amplifier arrangement as claimed in Claim 1, 2 or 3, characterized in that the differential amplifier includes a seventh and an eighth transistor of a second conductivity type opposite to the first conductivity type whose gate electrodes are coupled to the input terminals and whose source electrodes are coupled to a common terminal which is coupled by means of a second current source to a second supply terminal, and a ninth and a tenth transistor of the second conductivity type which are arranged in cascode with the seventh and the eighth transistor, respectively.

5. An amplifier arrangement as claimed in Claim 4, characterized in that the gate electrodes of the ninth and the tenth transistor are coupled together and in that an eleventh transistor of the second conductivity type is arranged between the common terminal of the source electrodes of the seventh and the eighth transistor and the common gate electrode of the ninth and the tenth transistor, the drain electrode of said eleventh transistor being connected to its gate electrode and to the first supply terminal by means of a third current source.

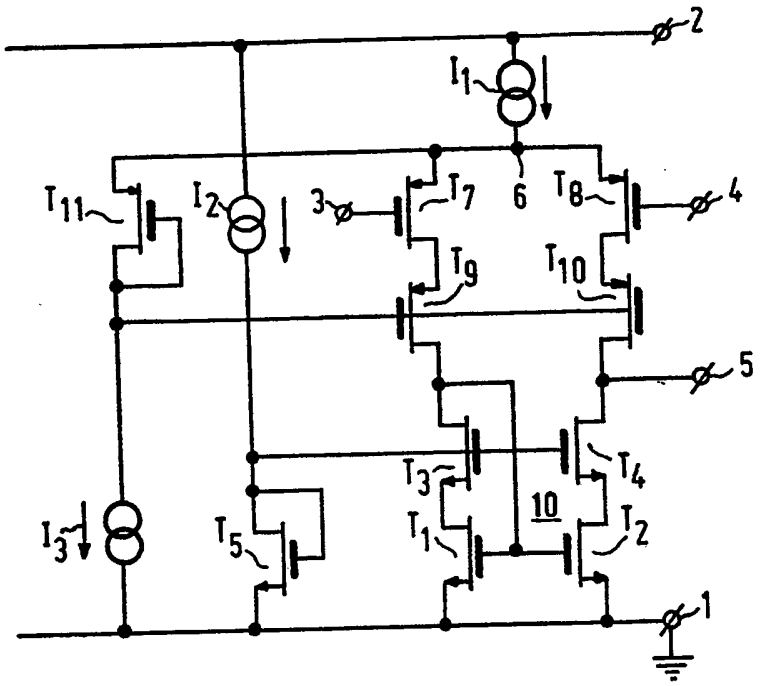
6. An amplifier arrangement as claimed in Claim 5, characterized in that a twelfth transistor of the first conductivity type is arranged in series with the eleventh transistor, said twelfth transistor having its source electrode coupled to the common gate electrode of the ninth and the tenth transistor and having its gate electrode coupled to the second supply terminal.

7. An amplifier arrangement as claimed in Claim 5 or 6, characterized in that the third current source is constituted by a thirteenth transistor of the first conductivity type whose source electrode is coupled to the first supply terminal and whose gate electrode is coupled to the gate electrode of the fifth transistor.

8. An amplifier arrangement as claimed in Claim 4, characterized in that the arrangement is formed as an integrated circuit on a substrate of a first conductivity type in which the seventh and the eighth transistor are arranged in a zone of a second conductivity type which is connected to the second supply terminal and in which the ninth and the tenth transistor are arranged in separate zones of the second conductivity type which are connected to the source electrodes of the seventh and the eighth transistor, respectively, and in that the gate electrodes of the ninth and the tenth transistors are connected to the gate electrodes of the seventh and the eighth transistor, respectively.

9. An amplifier arrangement as claimed in Claim 4, characterized in that the arrangement is formed as an integrated circuit on a substrate of a first conductivity type in which the seventh and the eighth transistor are arranged in a zone of a second conductivity type which is connected to the second supply terminal and in which the ninth and the tenth transistor are arranged in a common zone of the second conductivity type which is connected to the common terminal of the source electrodes of the seventh and the eighth transistor, and in that the gate electrodes of the ninth and the tenth transistor are connected to the gate electrodes of the seventh and the eighth transistor, respectively.

10. An amplifier arrangement as claimed in Claim 4, characterized in that the arrangement is formed as an integrated circuit on a substrate of a first conductivity type in which the seventh and the eighth transistor are arranged in a zone of a second conductivity type whichis connected to the second supply terminal and in whichthe ninth and the tenth transistor are arranged in a common zone of the second conductivity type which is connected to the common terminal of the source electrodes of the seventh and the eighth transistor, and in that the gate electrode of the ninth transistor is connected to the gate electrode of the tenth transistor and to the gate electrode of the seventh transistor.


2
I1
T11
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6
T8
4
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5
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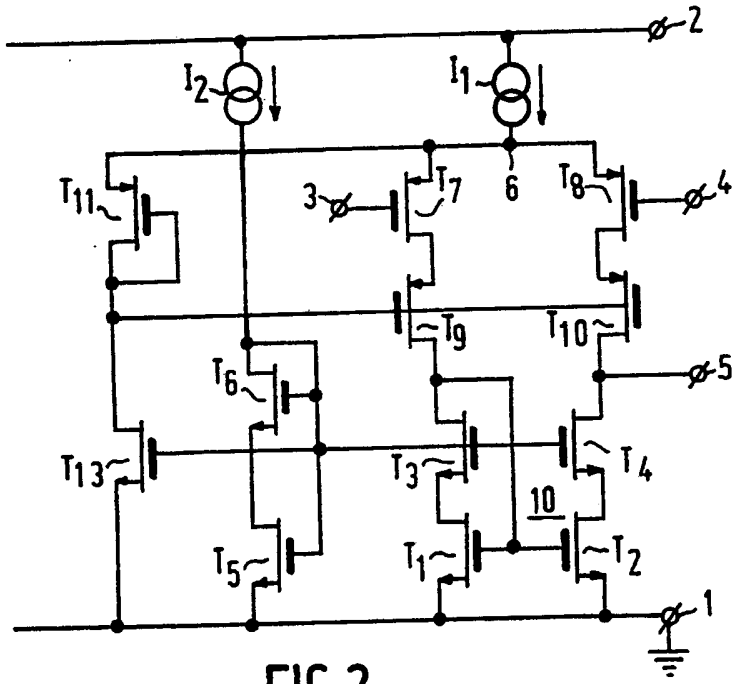
FIG.1


2
I2
I1
T11
3
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T8
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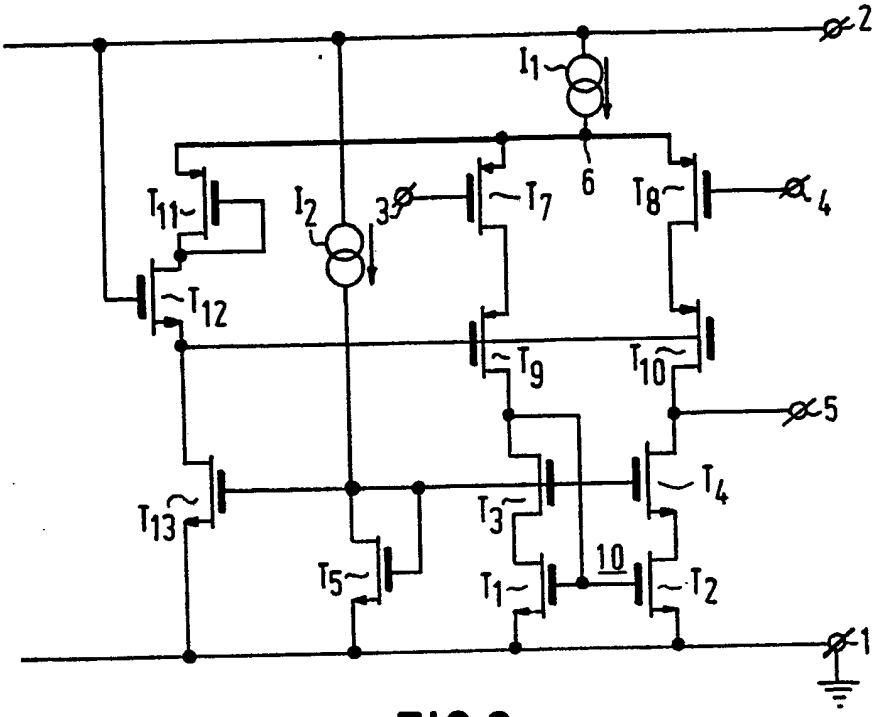
FIG.2


2
I1
6
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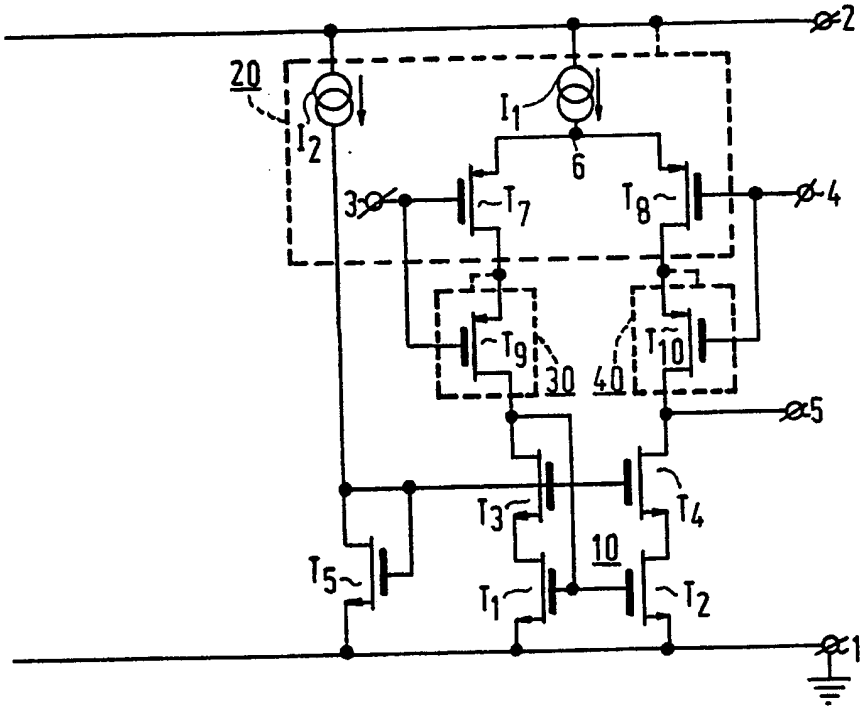
4
T12
T9
T10
5
T13
T4
T3
T5
10
T1
T2
1

FIG.3


2
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I2
I1
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3
T7
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30
40
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5
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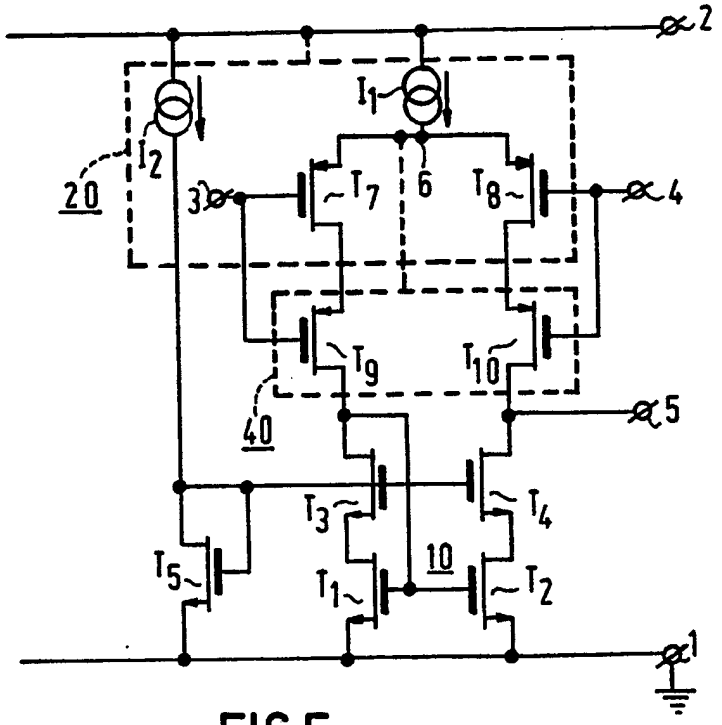
FIG.4


2
I1
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T7
6
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40
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T3
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T5
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FIG.5

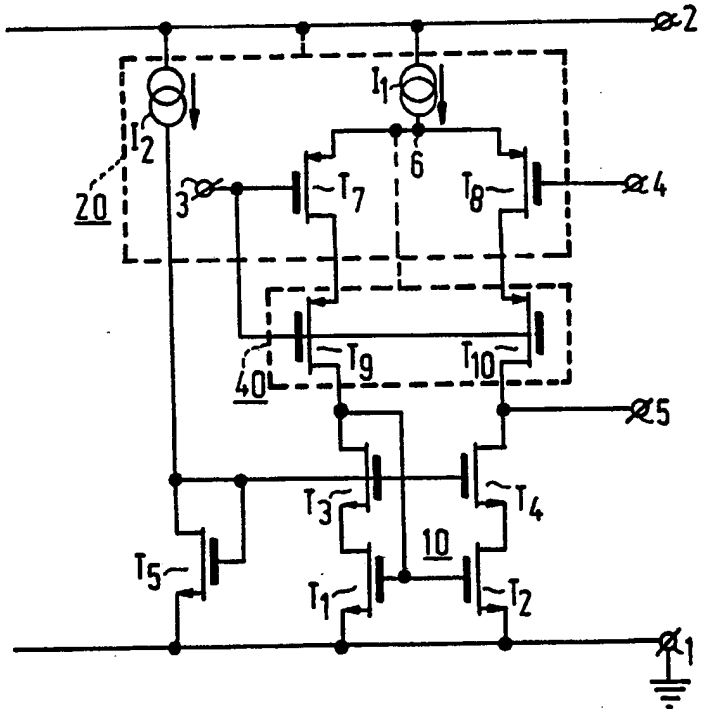
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FIG.6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 20 1898

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-22, no. 3, June 1987, pages 330-334, IEEE, New York, US; J.A.FISHER et al.: "A highly linear CMOS buffer amplifier" * Pages 330-334, especially figures 1,4,8; paragraph I.: "introduction", paragraph II.: "Circuit description", A. "Input Stage" * ---	1,4	H 03 F 3/45
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-17, no. 6, December 1982, pages 969-982, IEEE, New York, US; P.R.GRAY et al.: "MOS operational amplifier design - A tutorial overview" * Pages 969-982, especially figure 16; page 977, left-hand column, lines 11-15 * ---	4,5	
A	ELECTRONICS, vol. 44, no. 2, 18th January 1971, pages 81-84, New York, US; D.C.WYLAND: "FET cascode technique optimizes differential amplifier performance" * Pages 81-84, especially figure 3a; page 82, paragraph: "Quasi-cascode configuration" * ---	8	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 03 F
A	FR-A-2 588 707 (S.G.S. MICROELETTRONICA) * Figures 2,4; page 9, line 23 - page 11, line 20 * -----	4,8-10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12-12-1988	TYBERGHIEN G.M.P.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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